Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT A-**
2. **INPUT A+**
3. **OFFSET NULL A**
4. **V-**
5. **OFFSET NULL B**
6. **INPUT B+**
7. **INPUT B-**
8. **OFFSET NULL B**
9. **V+ (B)**
10. **OUTPUT B**
11. **OUTPUT A**
12. **V+ (A)**
13. **OFFSET NULL A**

**.061”**

**.039”**

**2 1 13**

**7 8**

**X**

**3**

**4**

**5**

**6**

**12**

**11**

**10**

**9**

**7**

**4**

**7**

**DIE ID**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0034” X .0034”**

**Backside Potential: FLOATING (or V-)**

**Mask Ref: X**

**APPROVED BY: DK DIE SIZE .039” X .061” DATE: 10/4/22**

**MFG: NATIONAL THICKNESS .013” P/N: LM747**

**DG 10.1.2**

#### Rev B, 7/19/02